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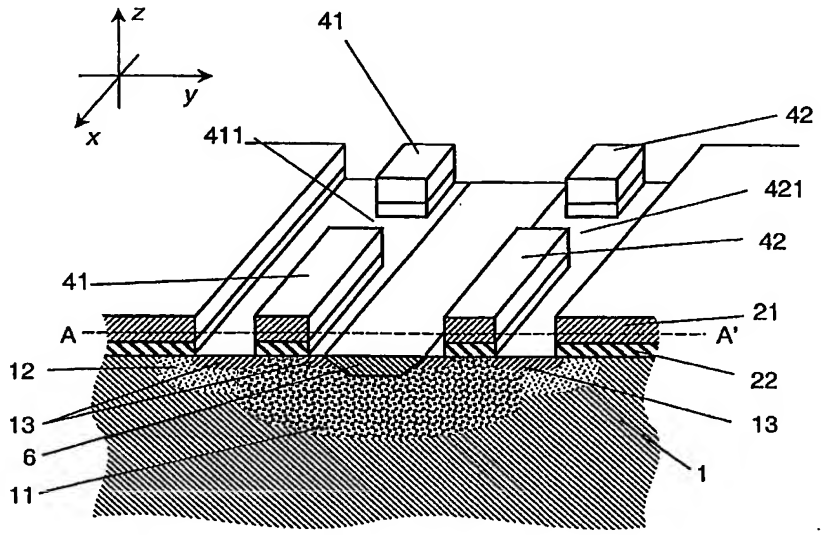
(54) Title: INSULATED GATE SEMICONDUCTOR DEVICE AND METHOD OF MAKING THE SAME



(57) Abstract: An insulated gate semiconductor device comprising a semiconductor substrate (1) having a top surface and an insulated gate (21,22) formed on the top surface from a layered structure (2) that comprises at least one electrically insulating layer (22), wherein at least one strip (41, 42) of the layered structure (2) is disposed on an area of the top surface between an edge of the insulated gate (21,22) and a first main contact (6). A manufacturing method for an insulated gate semiconductor device comprising the steps of forming a cell window (3) in said layered structure (2), forming at least one process mask (51) that partially covers the cell window (3) and extends to at least partially cover said at least one strip (41, 42) of the layered structure said at least one strip (41, 42) serving as an edge for the at least one process mast: (51).

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INSULATED GATE SEMICONDUCTOR DEVICE AND METHOD OF MAKING THE SAME

DESCRIPTION

Technical Field

The invention relates to the field of semiconductor devices. It relates in particular to a method for producing an insulated gate semiconductor device and an insulated gate semiconductor device as described in the preamble of claims 1 and 7, respectively.

Prior Art

To manufacture a cathode in a state-of-the art insulated gate bipolar transistor (IGBT) cell, a shallow base region and a source region are normally formed in a semiconductor substrate by means of a self-aligned process, wherein the source region is disposed in a portion of the base region. This is achieved by using a poly-silicon layer, which is to serve as a gate in the future device, as a hard mask for doping steps required in forming those regions, i.e. by doping through a cell window that has to be formed in the poly-silicon layer before the doping steps are carried out. Various topologies are common for IGBT cells, characterized by a shape of the cell window, which may be linear, circular, square, etc. In general, a plurality of cells is

formed on one common semiconductor substrate. However, if IGBT cells are required that have a size comparable to that of commonly available semiconductor wafers, only one single cell per semiconductor substrate may be formed. Doping is in general done by an implantation followed by a subsequent diffusion step, but may be done by diffusion and/or implantation alone or by other methods.

To provide IGBTs with an improved safe operating area (SOA), in particular for high voltage devices with ratings that exceed 2000V, a composite base region is often employed. The composite base region comprises a deep base region in addition to the shallow base region, where the shallow base region and the deep base region partially overlap one another, the deep base region being narrower and higher doped than the shallow base region, i.e. having a smaller dimension in at least one direction parallel to the poly-silicon layer. To add the deep base region, a doping mask that partially masks the cell window is therefore required. This doping mask has to be accurately aligned relative to the cell window if optimum device performance is to be achieved. Misalignment will lead to an uncontrollable shift in a threshold voltage and a potential reduction in SOA capability.

Another process step that requires accurate mask alignment is the formation of a source contact. If a contact mask is misaligned, a width of the source region between the source contact and a channel will deviate from a corresponding design value. However, if the width of the source region varies throughout the IGBT cell, a degradation of a short circuit capability will result.

Description of the Invention

It is an object of the invention to provide a method for manufacturing an insulated gate semiconductor device cell of the type mentioned initially that permits accurate alignment between a deep base region and/or a source contact on the one side and a source region and/or a shallow base region and/or a cell window on the other side and an insulated gate semiconductor device cell in which performance degradation due to misalignment, in particular source contact misalignment, will be reduced.

This object is achieved by a method according to claim 1 and a semiconductor device according to claim 7.

In the inventive method, a cell window is formed in a layered structure, said layered structure being disposed on a top surface of a semiconductor substrate, in such a manner that, inside the cell window, at least one strip of the layered structure remains. For subsequent process steps that require partial masking of the cell window, at least a first process mask is formed in such a way that at least one first strip acts as a first edge for said first process mask. This has the advantage that a position of a first process mask edge for the at least one additional subsequent process step is accurately defined relative to the cell window. Favourably, at least one additional layer, in particular an oxide layer or a primer for adding the process mask, may be disposed so that it at least partially covers the at least one strip and/or a main portion of the layered structure surrounding the cell window before the process mask is added.

In a preferred variation of the inventive method, at least a first strip is formed as isolated strip, i.e. is not in touch with a main portion of the layered structure surrounding the cell window. If the layered structure comprises at least one electrically conducting layer, no electrical connection will therefore remain between a first, main portion of the electrically conducting layer that surrounds the cell window and a second portion of the electrically conducting layer comprised by the first strip. The second portion of the electrically conducting layer will therefore not be electrically active when the device is in operation. This has the advantage of improving process sensitivity for potential gate-emitter short problems during a subsequent etch step required for a formation of an emitter contact when manufacturing IGBT cells.

In a preferred variation of the inventive method, the first process mask serves as a doping mask for adding a deep base region. The deep base region is formed by doping with the doping mask present, with dopants of a first conductivity type, preferably by implantation with subsequent diffusion. This has the advantage that the deep base region is accurately aligned relative to the first strip. Preferably, the doping mask is subsequently removed and a shallow base region and a source region is formed in subsequent process steps, preferably by implantation with subsequent diffusion of dopants of the first and of a second conductivity type,

respectively. The deep and shallow base regions and the source region will thus be accurately aligned relative to one another.

In another preferred embodiment of the inventive method, the first process mask serves as a contact mask. A source region is added by doping through the cell window with dopants of the second conductivity type before the contact mask is formed. A first main contact is then formed by etching through the source region once the contact mask is in place. Accurate alignment of the first main contact within the cell window results.

In another preferred variation of the inventive method, the first process mask serves as doping mask. After removal of the first process mask and a number of intermediate process steps, a second process mask is added in such a way that the strip again acts as an edge for said second process mask, which preferably serves as contact mask.

In another preferred variation of the method according to the invention, one or more, preferably all, strips are removed in a subsequent process step.

In the inventive semiconductor device according to claim 7, at least one strip of a layered structure is disposed on a third area of a top surface of a semiconductor substrate between a gate edge and a first main contact. This has the advantage that a degradation of short circuit capabilities resulting from potential misalignment of the first main contact relative to the gate edge will be reduced compared to a state of the art semiconductor device.

In a preferred embodiment of the inventive semiconductor device, a second portion of an electrically conducting layer of the layered structure, said second portion of the electrically conducting layer being comprised by the at least one strip, is electrically connected to a first main contact. This way, a degradation of short circuit capabilities resulting from misalignment can be eliminated completely.

Further advantageous realizations can be found in the dependent claims.

Brief Explanation of the Figures

The invention will be explained in more detail in the following text with reference to exemplary realizations and in conjunction with the figures, in which:

Fig. 1 shows a cross section of a semiconductor substrate with a layered structure disposed on a top surface,

Figs. 2, 3, 4 and 5 illustrate how to manufacture an IGBT cell cathode,

Fig. 6 shows a IGBT cell cathode resulting from the manufacturing process shown in Figs. 2 through 5,

Fig. 7 shows a cut through the structure shown in Fig. 6, and

Figs. 8 and 9 show an insulated gate semiconductor device according to the invention.

The reference signs used in the figures are explained in the list of reference signs. In principle, identical reference symbols are used to denote identical parts.

Approaches to Realization of the Invention

Fig. 1a shows a cross section of an n-doped semiconductor substrate 1. A layered structure 2 comprising an oxide layer 22 and a poly-silicon layer 21 was disposed on a top surface of the semiconductor substrate 1. Figs. 2, 3, 4 and 5 illustrate how to manufacture an IGBT cell cathode in the semiconductor substrate 1: In a first step, a cell window 3 is generated in the layered structure 2 as shown in a perspective representation in Fig. 2 and in cross-section in Fig. 3a. Standard methods known to a person skilled in the art of photolithography are preferably used to remove the layered structure 2 where desired. The cell window 3 is formed in such a way that a first row of isolated strips 41 and a second row of isolated strips 42 of the layered structure 2 remain inside the cell window 3, so that at least one opening 411 and 421 results within each row. A second portion of the poly-silicon layer 21 comprised by the isolated strips 41, 42 is not electrically connected to a first, main portion of the

poly-silicon layer 21 that surrounds the cell window 3, and will therefore not be electrically active when the device is in operation. This has the advantage of improving a process sensitivity for potential gate-emitter short problems during a subsequent contact etch.

A first process mask 51, typically photoresist, is then formed so that said first process mask 51 partially covers the cell window 3, and at least partially covers each of the strips 41 and 42 as shown in Fig. 3b. Widths w_1 and w_2 are preferably bigger than a typical uncertainty in the position of the process mask 51, i.e. w_1 and w_2 measure preferably a few micrometers, preferably 2 to 3 micrometers. A deep p^+-base region 11 as shown in Fig. 3d is then formed by a first ion implantation step and a subsequent first diffusion step of dopants of a first conductivity type, e.g. Boron. This will provide the resulting IGBT cell with good safe operating area (SOA) capabilities. During the ion implantation step, the strips 41, 42 act as a process mask edge. A resulting first implantation profile 11a as shown in Fig. 3c is therefore laterally confined by the strip position. The first process mask 51 can now be removed for further processing steps.

Additional processing steps are required to complete the IGBT cell. A shallow p-base region 12 with dopants of the first conductivity type as shown in Fig. 4b is added, again by a second implantation step, resulting in a second implantation profile 12a as shown in Fig. 4a. This time, implantation is done over the whole cross section of the cell window 3. After a second diffusion step, the shallow p-base region 12 results. In a subsequent step, an n^+-source region 13 with dopants of a second conductivity type, e.g. Arsenic or Phosphorus as shown in Fig. 4c is added preferably by a third implantation step followed by a third diffusion step.

In a preferred embodiment of the invention, a second process mask 52 is then formed as shown in Fig. 5a. In a subsequent contact etch step, the second process mask 52 serves as a contact mask, with the strips 41 and 42 again acting as mask edges. An emitter contact 6 is formed by etching through the n^+-source region 13 in an area between the strips 41 and 42, as shown in Fig. 5b, and by filling a resulting contact well with metal, so that a good electrical connection is established between the emitter contact 6 and the deep p+-base region 11.

A IGBT cell cathode resulting from the manufacturing process described above in connection with Figs. 2 through 5 is shown in Fig. 6. The structure shown is a so-called mini-strip design. Fig. 7a shows a cut through the structure of Fig. 6, along the line A-A' and perpendicular to the *z*-axis. An alternative design, a so-called full-strip design is shown in Fig. 7b. The openings 411 and 421 ensure that an outer portion of the n+-source regions 13 located between each of the strips 41, 42 and the first, main portion of the layered structure 2 surrounding the cell window 3 are electrically connected to the emitter contact 6 via a distributed resistance that is in series with the emitter contact 6, as known from emitter ballasting. The ration of the openings to the full strip lengths is an important factor in the design of a IGBT cell. The basic idea behind this approach is that if an emitter current increases locally, the voltage drop across an emitter ballast resistance will also increase, which in turn will reduce the emitter current and divert the emitter current to other regions of the n+-source region 13. This has the advantage that it promotes a more uniform current distribution.

In another preferred embodiment of the invention, an electrical connection is established between the emitter contact 6 and the second portion of the poly-silicon layer 21 comprised by the strips 41, 42. This is preferably achieved by also etching away such portions of the strips 41, 42 that are not covered by the contact mask 52 during the contact etch step, and choosing a thickness of the emitter contact 6 appropriately.

In another preferred embodiment of the invention, the strips 41 and 42 are removed by a dry-etch step after the deep p^+-base region 11 has been formed. A dry-etch mask is formed on those portions of the poly-silicon layer 21 that are not to be removed by the dry-etch step, in particular the first, main portion of the poly-silicon layer 21 surrounding the cell window 3, i.e. the future gate regions. This is of particular advantage in another preferred variant of the method according to the invention, in which the cell window 3 in the layered structure is formed in such a manner that the strip that remains forms a closed loop, which may, e.g., be rectangular, circular, hexagonal, etc.

A vertical cut through an insulated gate semiconductor device according to the invention is shown in Fig. 8. The device represents an IGBT structure, with a p-

doped anode region 14 formed on the bottom of the semiconductor substrate 1, said p-doped anode region 14 being electrically connected to an anode electrode 7. A low temperature oxide layer 8 is disposed on top of and around the poly-silicon layers 21, electrically insulating poly-silicon layer 21 from the emitter metallization 9. In this embodiment, there is no electrical connection between the strips 41, 42 of the second portion of the poly-silicon layer 21 and either the emitter metallization 9 or the emitter contact 6. Another vertical cut through one of the openings in the strips of the semiconductor device according to the invention is shown in Fig. 9.

In a preferred embodiment of the semiconductor device according to the invention an electrical connection exists between the second portion of the poly-silicon layer 21 being comprised by the strips 41, 42 and the emitter metallization 9 and the emitter contact 6.

List of Reference Signs

1	Semiconductor substrate
11	First doped region, deep p^+-base
11a	First implantation profile
12	Second doped region, shallow p-base
12a	Second implantation profile
13	Third doped region, n^+-source
14	p-doped anode region
21	Electrically conducting layer, polysilicon layer
22	Electrically insulating layer
3	Cell window
41, 42	First, second strips
411, 421	First, second opening
51	First process mask, doping mask
52	Second process mask, contact mask
6	First main contact, emitter contact
7	Anode metallization
8	Low temperature oxide
9	Cathode metallization

PATENT CLAIMS

1. Method to produce an insulated gate semiconductor device cell, comprising the steps of

   - forming a cell window (3) in a layered structure (2) on a cathode side of a semiconductor substrate (1), said layered structure comprising an oxide layer (22) on top of said semiconductor substrate (1) and a poly-silicon layer (21) on top of said oxide layer (22),
     said cell window being formed by partially removing said layered structure down to the substrate, leaving at least two isolated strips (41, 42) of the layered structure to remain within the cell window,
     said isolated strips (41, 42) dividing the cell window (3) in an outer cell window region located between the isolated strips and the outer edge of the cell window and an inner cell window region located between the isolated strips;
   - forming doped regions (11, 12) in the semiconductor substrate by applying a process mask to the inner or outer cell window region respectively and implanting dopants into the substrate through the other, uncovered cell window region;

   characterized in, that

   - in or after the cell window forming step, openings (411, 421) in the isolated strips (41, 42) are formed by further removing some of said layered structure down to the substrate, and that
   - a doped region (13) in the semiconductor substrate beneath the openings (411, 421) is formed by implanting dopants into the substrate through the openings (411, 421).

2. An insulated gate semiconductor device, comprising

- a layered structure (2) on an essentially planar cathode side of a semiconductor substrate (1), said layered structure being arranged around a cell window (3) and forming an insulated gate comprising an oxide layer (22) on top of said semiconductor substrate (1) and a poly-silicon layer (21) on top of said oxide layer (22),
- a first doped region (11) of a first conductivity type extending into the substrate beneath the centre of said cell window (12),
- a second doped region (12) of a first conductivity type, in particular a shallow base region (12), extending into the semiconductor substrate beneath the outer edge of the cell window adjacent said first doped region (11);
- at least one third doped region (13) of a second conductivity type, in particular a source region (13), extending partially into said second doped region (12) adjacent said first doped region (11); and
- a first main contact (6) disposed on the top surface electrically connected to said first doped region (11) and said third doped region (13);

characterized in that

- at least two isolated strips (41, 42) are arranged in the cell window (3) between the insulated gate (21) and the first main contact (6), dividing the cell window (3) in an outer cell window region and an inner cell window region, said outer cell window region being located between the isolated strips and insulated gate (21) and above the third doped region (13), and said inner cell window region being located between the isolated strips and comprising the main contact (6),
  said strips comprising an oxide layer on top of the semiconductor substrate and a poly-silicon layer on top of the oxide layer, that
- the two strips comprise openings (411, 421), and that
- the third doped region (13) extends into the substrate beneath the openings, electrically connecting the third doped region (13) beneath the outer cell window region to the first main contact (6).

3. An insulated gate semiconductor device as in claim 2, characterized in, that

   - the ratio length of openings (411, 421) to lengths of strips is laid out to match a desired emitter ballast resistance.

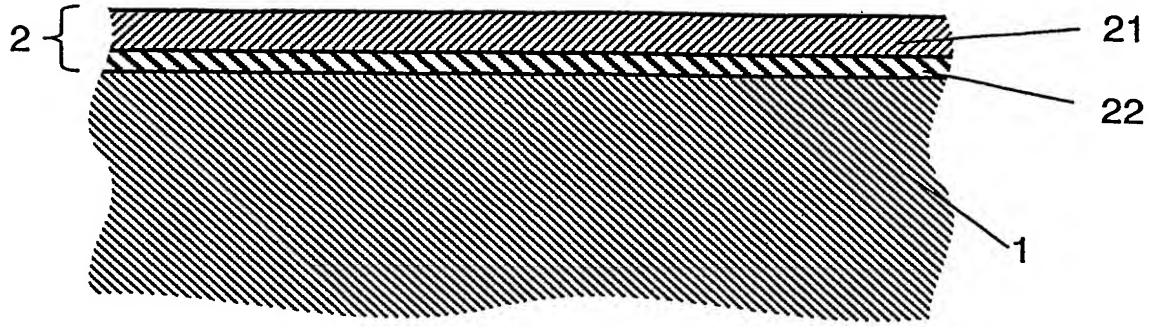

Fig. 1

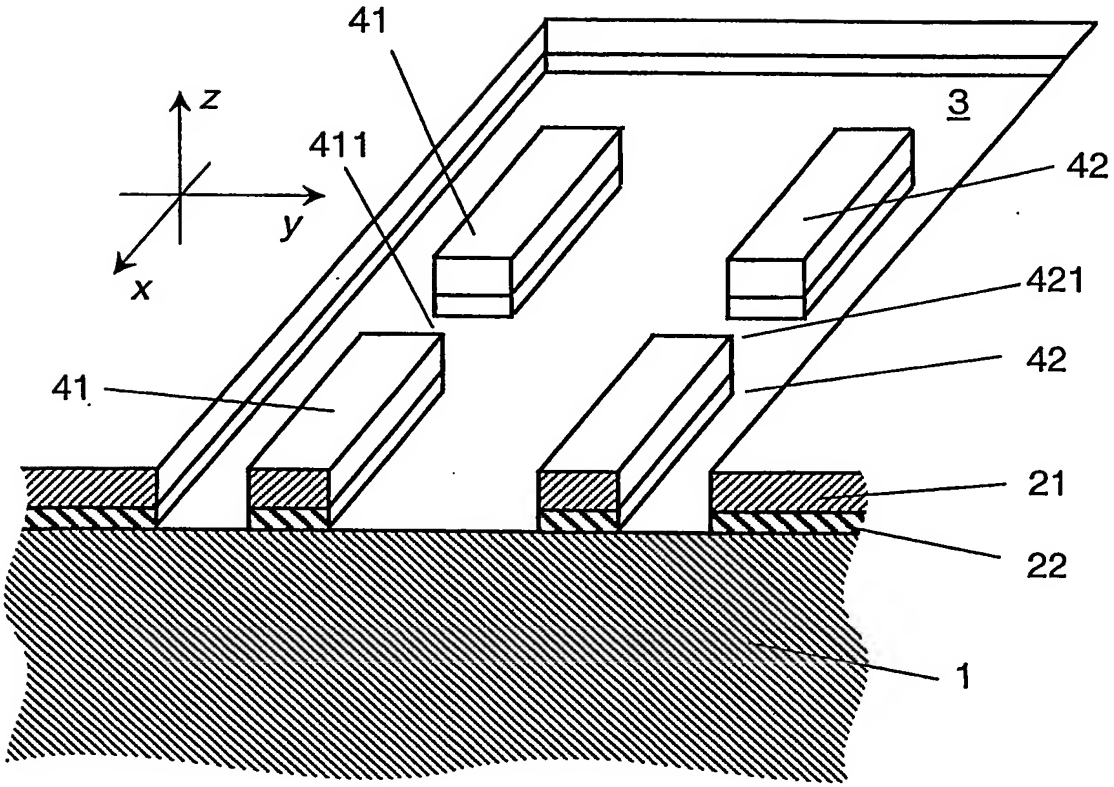

Fig. 2

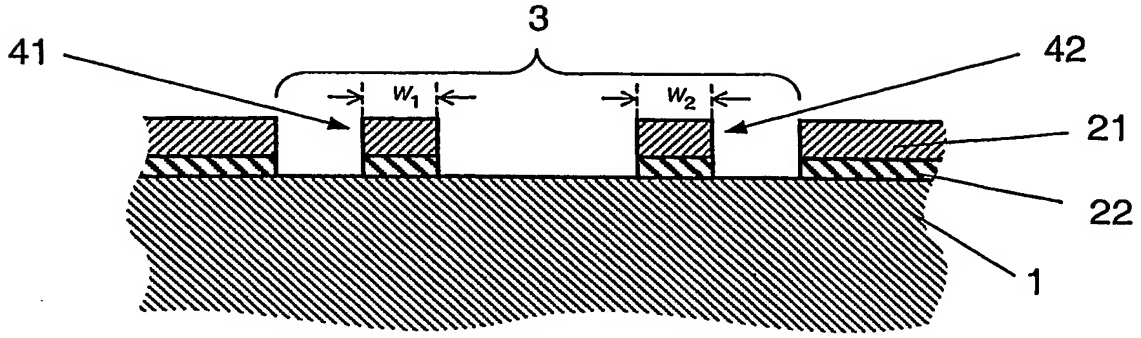

Fig. 3a

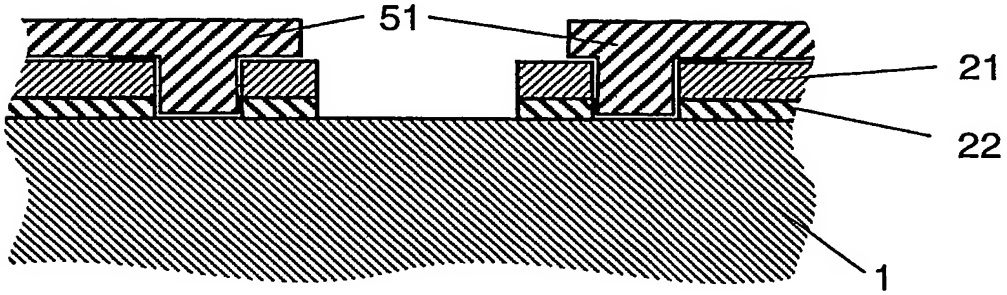

Fig. 3b

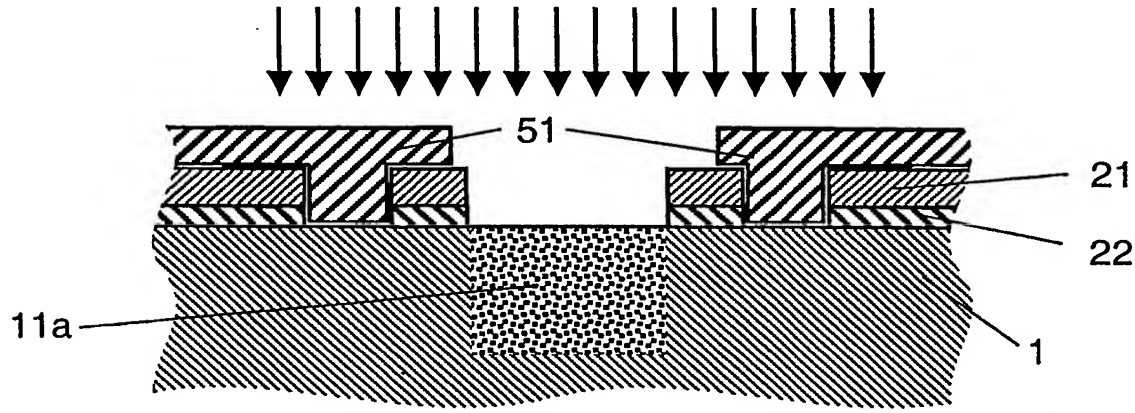

Fig. 3c

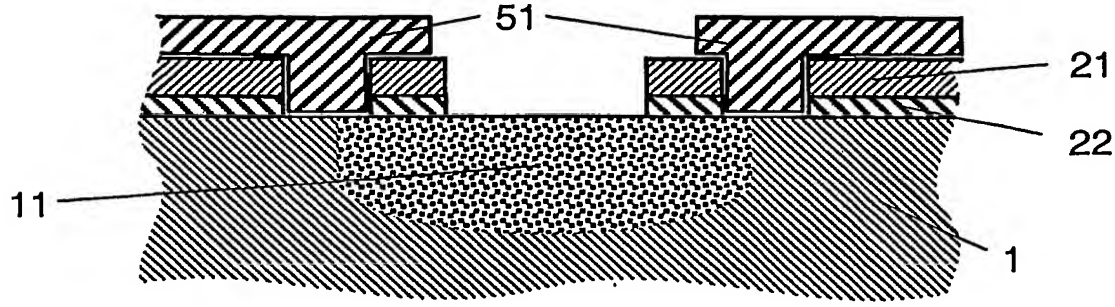

Fig. 3d

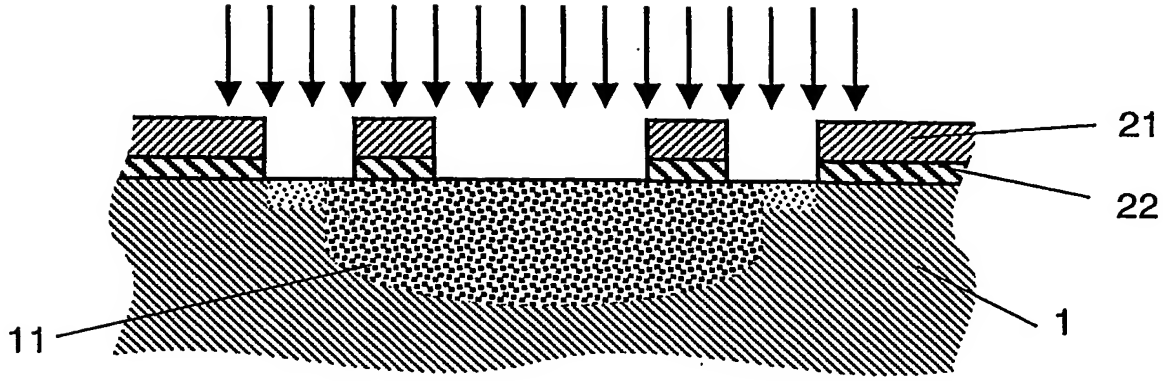

Fig. 4a

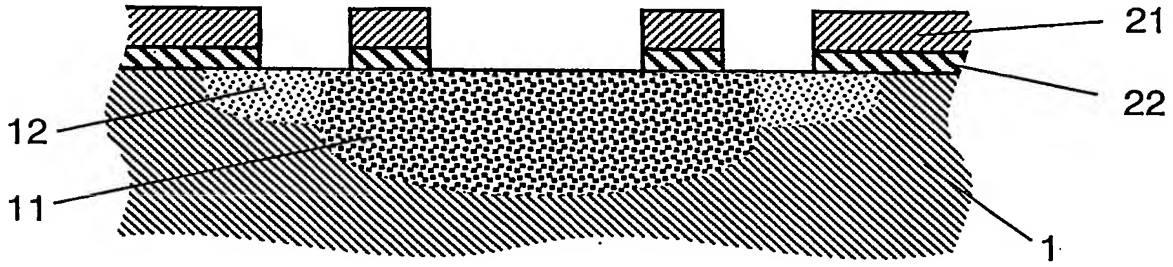

Fig. 4b

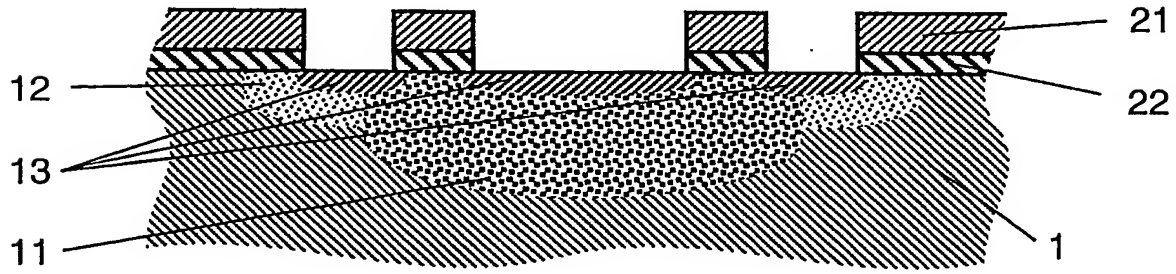

Fig.4c

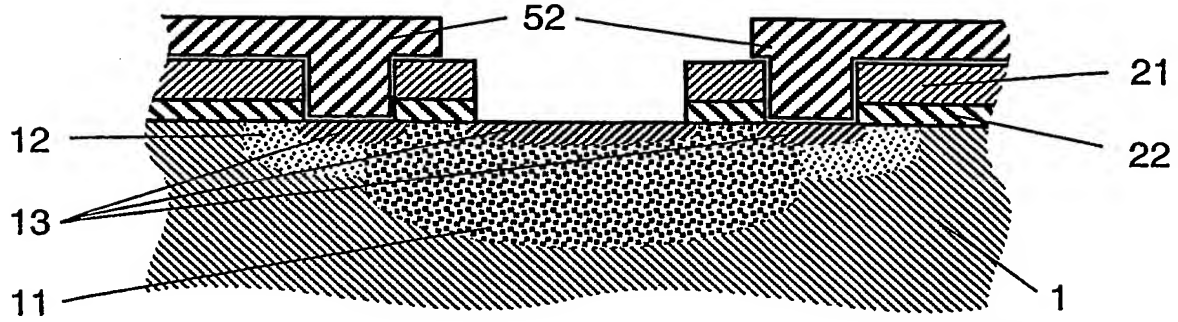

Fig. 5a

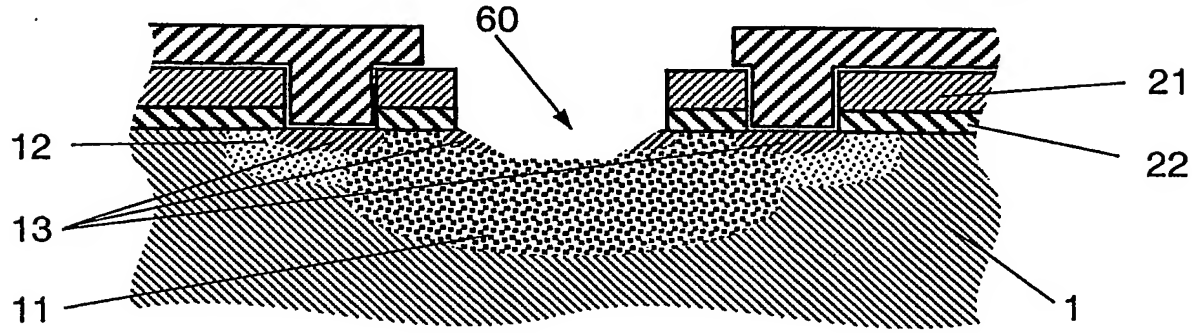

Fig. 5b

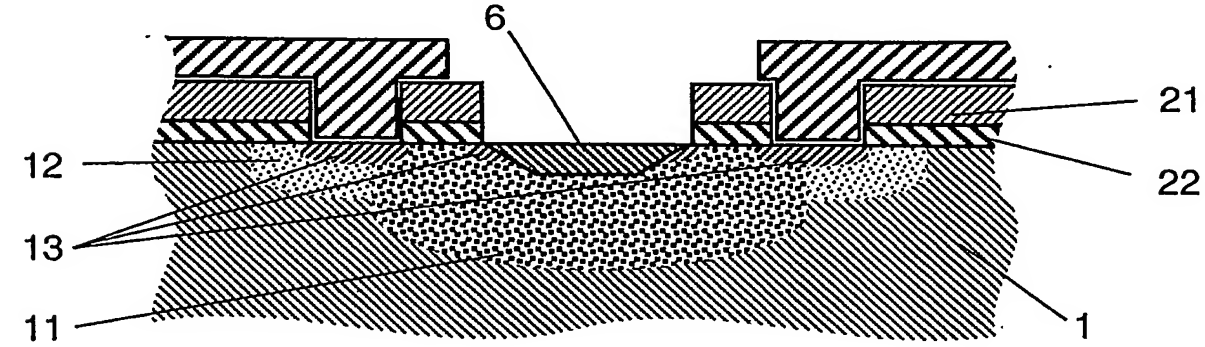

Fig. 5c

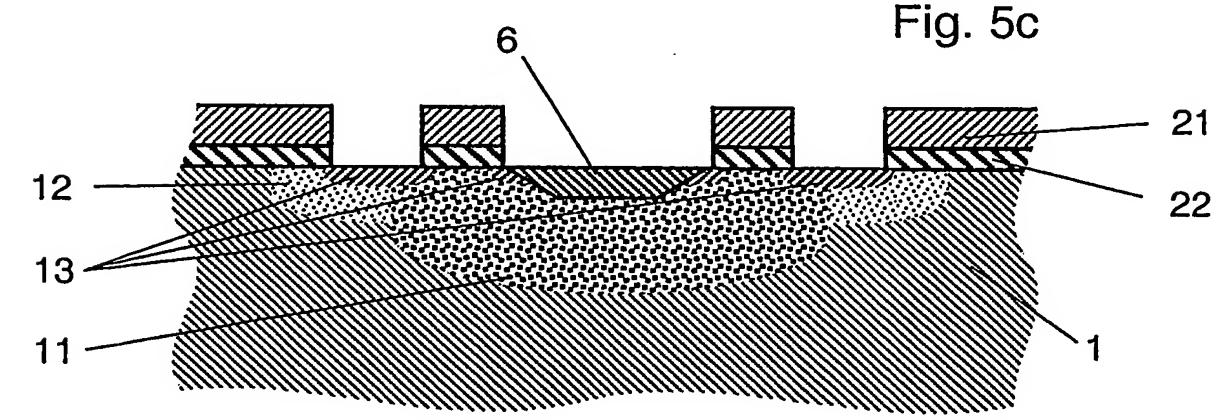

Fig. 5d

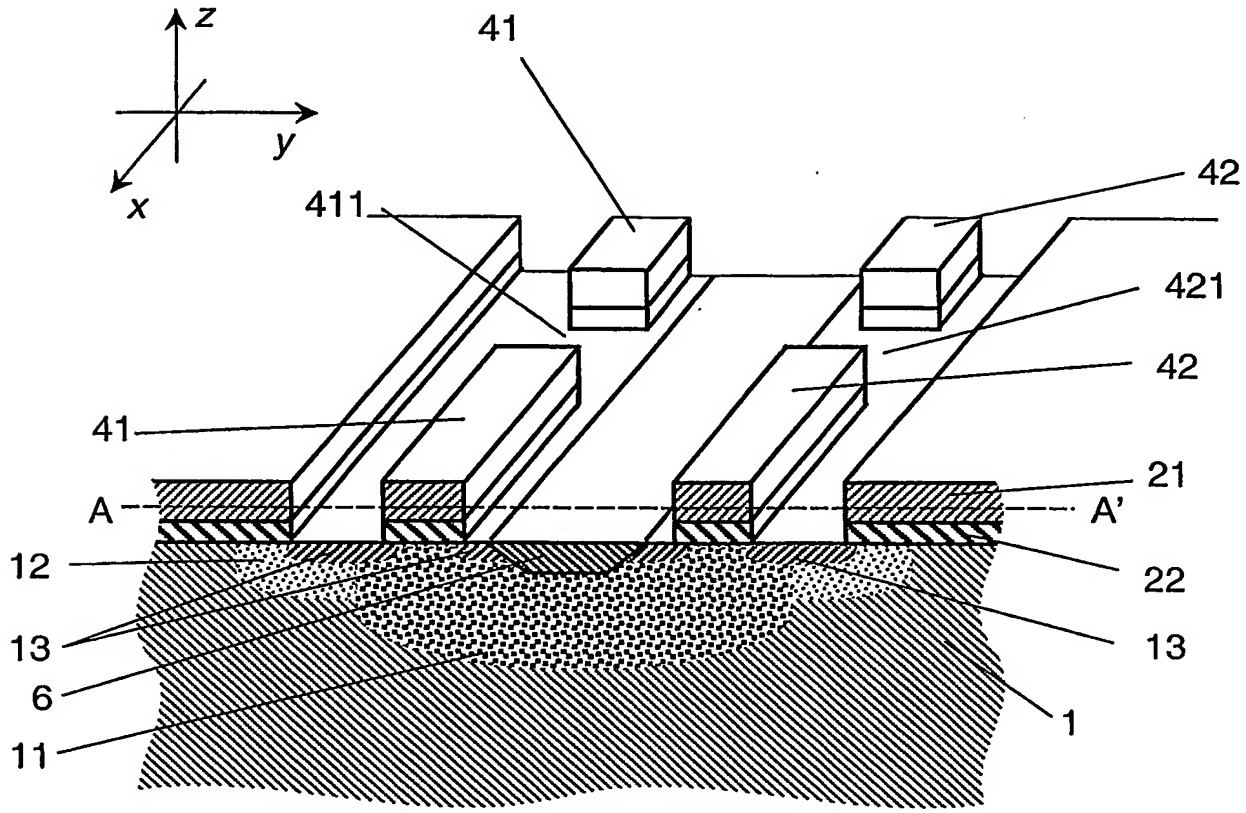

Fig. 6

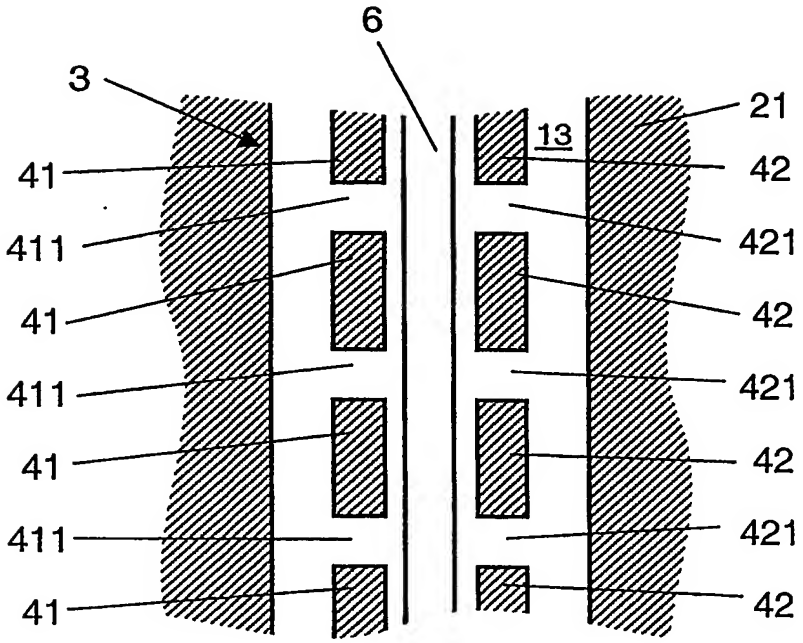
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Fig. 7a

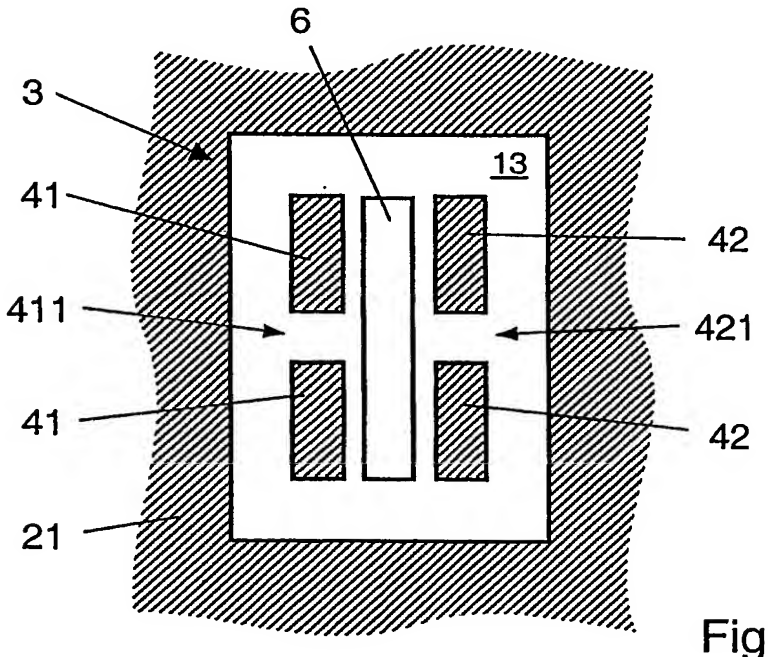
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Fig. 7b

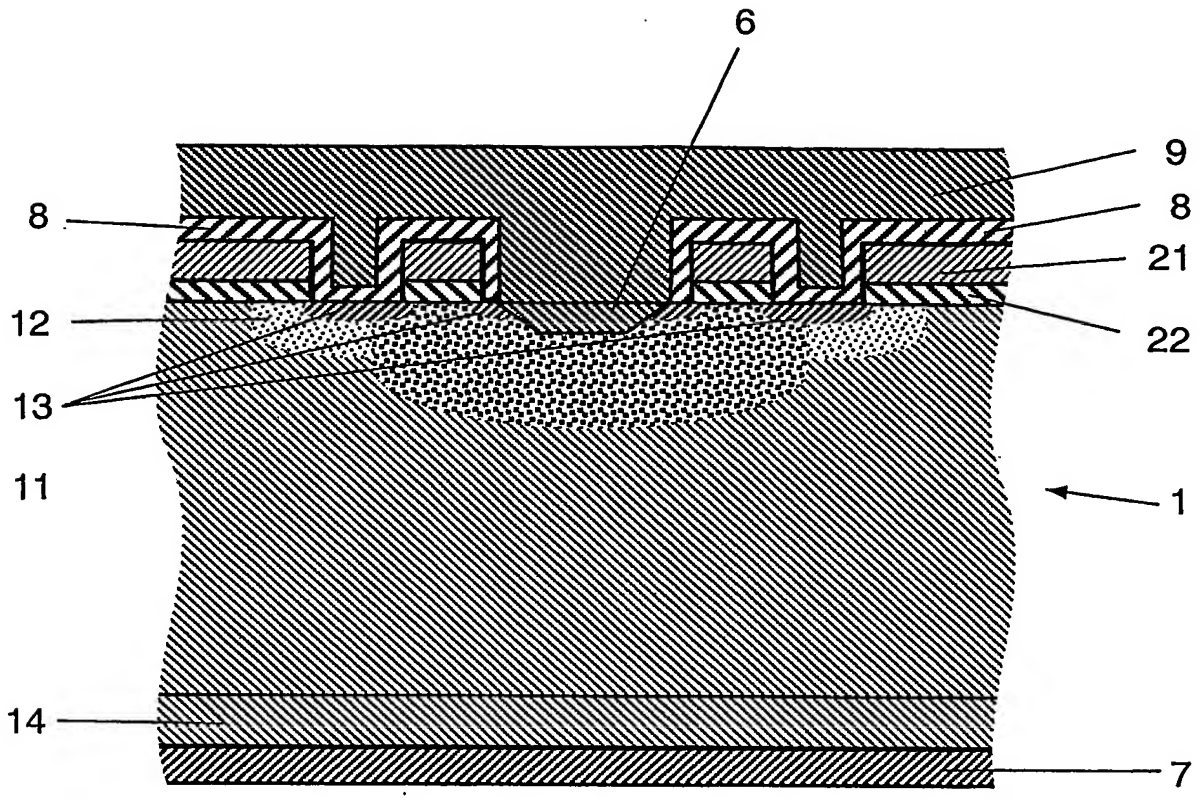

Fig. 8

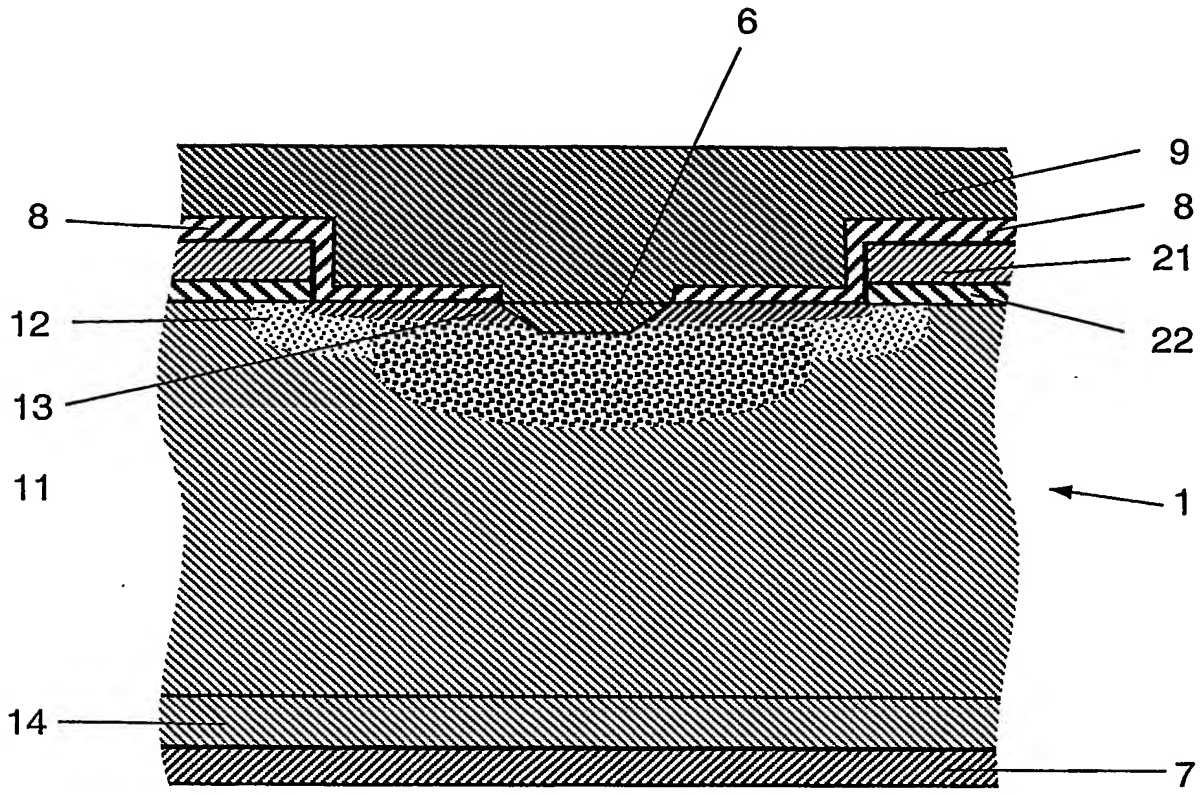

Fig. 9

INTERNATIONAL SEARCH REPORT

International Application No
PCT/CH 03/00809

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/739 H01L21/331 H01L29/423 H01L29/417

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 012, no. 069 (E-587), 3 March 1988 (1988-03-03) -& JP 62 211955 A (MITSUBISHI ELECTRIC CORP), 17 September 1987 (1987-09-17) abstract; figures 1A-1I	1,2
A	PATENT ABSTRACTS OF JAPAN vol. 012, no. 099 (E-594), 31 March 1988 (1988-03-31) -& JP 62 229977 A (TOSHIBA CORP), 8 October 1987 (1987-10-08) abstract; figures 1A-1D,2A-2D	1,2
A	US 5 703 383 A (NAKAYAMA K) 30 December 1997 (1997-12-30) column 10, line 65 -column 11, line 28; figures 11,12	1-3

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
18 February 2004	26/02/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Morvan, D

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter[illegible]lication No
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